



PATENT
Conf. No.: 7556

IN THE UNITED STATES PATENT OFFICE

Applicants: Jonathan B. Ballagh et al.
Assignee: Xilinx, Inc.
Title: Clock Stabilization Detection For Hardware Simulation
Serial No.: 10/600,848 File Date: June 19, 2003
Examiner: Andre Pierre Louis Art Unit: 2123
Docket No.: X-1192 US Conf. No.: 7556

Enter Per
RCE RMB
8-14-07

Mail Stop AF
COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450

Please
~~Do not ENTER~~
APL
7/14/07

AMENDMENT IN RESPONSE TO FINAL OFFICE ACTION

In response to the Final Office Action mailed from the Patent Office on
May 3, 2007, please replace/substitute the following claims as indicated.

Amendments to the Claims begin on page 2 of this paper.

Remarks begin on page 9 of this paper.